Integrated Protection Circuit Testing for an NMOS Silicon Carbide Gate Driver

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Background/Relevance

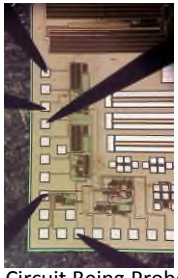
- Silicon carbide has been found to be an efficient material for manufacturing high temp, high voltage Power MOSFETs.
- Recently a low-voltage SiC gate driver has been developed to work laterally and be integrated into the power device process.

Innovation

- Use SiC to manufacture power device and gate driver on a single die to increase performance and reduce cost.
- Design protection circuitry to also be integrated into a single die design to ensure proper and continuous functionality.

Approach

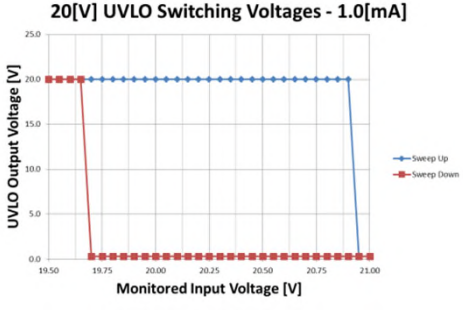
- Simulate Under Voltage Lockout (UVLO) and Current Desaturation (DESAT) circuits using Cadence.
- Perform Die Level testing on the circuits using a SemiProbe Station.
- Modify daughter printed circuit board (PCB) to accommodate SiC chip with total inclusive design.
- Populate the PCB with necessary resistors, capacitors, diodes, and SiC chip.
- Test entire system up to and exceeding 350°C.

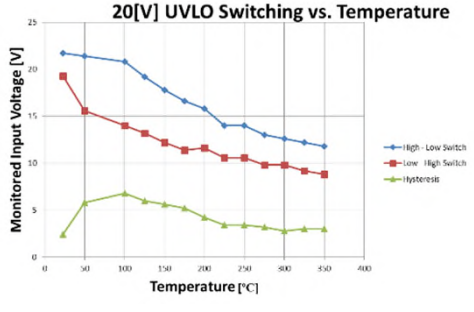

- Circuit Being Probed


- Assembled Daugheter PCB

Key Results

- Die level testing proved proper functionality of both UVLO and DESAT circuitry with desired voltage switching points.
- System level testing confirmed proper assembly and board design.
- Over temp testing showed continued functionality with decreasing switching voltages as expected.





Conclusions

- SiC provides improved performance over traditional Si integrated circuits for applications requiring high temperature and/or high voltage applications.
- Integrated circuits designed in SiC allow for proper integration of power devices, gate drivers, and protection circuits all on a single die.
- Operating integrated circuits at temperatures exceeding 350°C is possible using SiC.

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